WHAT IS CLAIMED IS:

1. A method for designing a routing pattern for electrical contacts on a printed circuit board, comprising the steps of:

arranging contacts in a contact array of rows and columns on the printed circuit board,

electrically connecting groups of n columns of the contacts to n-1 columns of vias disposed interstitially in a via array between the n columns of the contacts, thereby forming a major vertical routing channel between adjacent groups of n columns of the contacts and the n-1 columns of vias,

electrically connecting a first number of the vias to first electrical traces, and

routing the first electrical traces to an outside edge of the via array, where the first electrical traces are routed out of the via array through the major vertical routing channel.

2. The method of claim 1, wherein the step of forming the major vertical routing channel further comprises forming a plurality of major vertical routing channels.

3. The method of claim 1, further comprising the steps of:

electrically connecting groups of n rows of the contacts to n-1 rows of vias disposed interstitially in the via array between the n rows of the contacts, thereby forming a major horizontal routing channel between adjacent groups of n rows of the contacts and the n-1 rows of vias,

electrically connecting a second number of the vias to second electrical traces, and

routing the second electrical traces to the outside edge of the via array, where the second electrical traces are routed out of the via array through the major horizontal routing channel.

4. The method of claim 3, wherein the step of forming the major horizontal routing channel further comprises forming a plurality of major horizontal routing channels.

5. The method of claim 1, further comprising the step of forming a minor horizontal routing channel by placing a portion of the vias in the via array in a row near the outside edge of the via array, and routing third electrical traces to the outside edge of the via array through the minor horizontal routing channel.

6. The method of claim 1, further comprising the step of forming a minor vertical routing channel by placing a portion of the vias in the via array in a column near the outside edge of the via array, and routing fourth electrical traces to the outside edge of the via array through the minor vertical routing channel.

7. The method of claim 1, further comprising the steps of designating a portion of the contacts as signal contacts and arranging each of the signal contacts to be adjacent another of the signal contacts in groups of two within the contact array.

8. The method of claim 1, further comprising the steps of designating a first portion of the contacts as signal contacts, a second portion of the contacts as power contacts, and third portion of the contacts as ground contacts, and arranging each of the signal contacts to be adjacent to at least one of the power contacts and at least one of the ground contacts within the contact array.

9. The method of claim 1, wherein the step of arranging the contacts into an array further comprises arranging the contacts into an orthogonal contact array.

10. The method of claim 1, wherein n equals six.

11. A printed circuit board, comprising:
contacts in a contact array of rows and columns on the printed circuit board,
groups of n columns of the contacts electrically connected to n-1 columns of vias disposed interstitially in a via array between the n columns of the contacts,
a major vertical routing channel formed between adjacent groups of n columns of the contacts and the n-1 columns of vias,
first electrical traces electrically connected to a first number of the vias, and

the first electrical traces routed to an outside edge of the via array through the major vertical routing channel.

12. The printed circuit board of claim 11, further comprising a plurality of major vertical routing channels.

13. The printed circuit board of claim 11, further comprising:

groups of n rows of the contacts electrically connected to n-1 rows of vias disposed interstitially in the via array between the n rows of the contacts,

a major horizontal routing channel formed between adjacent groups of n rows of the contacts and the n-1 rows of vias,

second electrical traces electrically connected to a second number of the vias, and

the second electrical traces routed to the outside edge of the via array through the major horizontal routing channel.

14. The printed circuit board of claim 13, further comprising a plurality of major horizontal routing channels.

15. The printed circuit board of claim 11, further comprising:

a minor horizontal routing channel adjacent a portion of the vias in the via array that are connected to contacts in a row near the outside edge of the via array, and

third electrical traces routed to the outside edge of the via array through the minor horizontal routing channel.

16. The printed circuit board of claim 11, further comprising:

a minor vertical routing channel adjacent a portion of the vias in the via array that are connected to contacts in a column near the outside edge of the via array, and

fourth electrical traces routed to the outside edge of the via array through the minor vertical routing channel.

17. The printed circuit board of claim 11, wherein a portion of the contacts are signal contacts, and each of the signal contacts is adjacent another of the signal contacts in groups of two within the contact array.

18. The printed circuit board of claim 11, wherein a first portion of the contacts are signal contacts, a second portion of the contacts are power contacts, and a third portion of the contacts are ground contacts, and each of the signal contacts is adjacent to at least one of the power contacts and at least one of the ground contacts within the contact array.

19. The printed circuit board of claim 11, wherein n equals six.

20. The printed circuit board of claim 11, wherein the vias in the via array are disposed interstitially and diagonally between the contacts.

21. The printed circuit board of claim 11, wherein the contacts at a perimeter of the contact array are signal contacts.

22. An integrated circuit package substrate, comprising:
contacts in a contact array of rows and columns on the integrated circuit package substrate,
groups of n columns of the contacts electrically connected to n-1 columns of vias disposed interstitially in a via array between the n columns of the contacts,
a major vertical routing channel formed between adjacent groups of n columns of the contacts and the n-1 columns of vias,
first electrical traces electrically connected to a first number of the vias, and
the first electrical traces routed to an outside edge of the via array through the major vertical routing channel.

23. The integrated circuit package substrate of claim 22, further comprising a plurality of major vertical routing channels.

24. The integrated circuit package substrate of claim 22, further comprising:

groups of n rows of the contacts electrically connected to n-1 rows of vias disposed interstitially in the via array between the n rows of the contacts,

a major horizontal routing channel formed between adjacent groups of n rows of the contacts and the n-1 rows of vias,

second electrical traces electrically connected to a second number of the vias, and

the second electrical traces routed to the outside edge of the via array through the major horizontal routing channel.

25. The integrated circuit package substrate of claim 24, further comprising a plurality of major horizontal routing channels.

26. The integrated circuit package substrate of claim 22, further comprising:

a minor horizontal routing channel adjacent a portion of the vias in the via array that are connected to contacts in a row near the outside edge of the via array, and

third electrical traces routed to the outside edge of the via array through the minor horizontal routing channel.

27. The integrated circuit package substrate of claim 22, further comprising:

a minor vertical routing channel adjacent a portion of the vias in the via array that are connected to contacts in a column near the outside edge of the via array, and

fourth electrical traces routed to the outside edge of the via array through the minor vertical routing channel.

28. The integrated circuit package substrate of claim 22, wherein a portion of the contacts are signal contacts, and each of the signal contacts is adjacent another of the signal contacts in groups of two within the contact array.

29. The integrated circuit package substrate of claim 22, wherein a first portion of the contacts are signal contacts, a second portion of the contacts are power contacts, and a third portion of the contacts are ground contacts, and each of the signal

contacts is adjacent to at least one of the power contacts and at least one of the ground contacts within the contact array.

30. The integrated circuit package substrate of claim 22, wherein n equals six.

31. The integrated circuit package substrate of claim 22, wherein the vias in the via array are disposed interstitially and diagonally between the contacts.

32. The integrated circuit package substrate of claim 22, wherein the contacts at a perimeter of the contact array are signal contacts.